FPGA Based Electronic Power ConditionersforSSPAsof Flexible Satellite payloads

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Abstract*—Electronic Advances in radiation hardened FPGAs has potential of unfolding several new avenues for space applications. The reach of these devices is found to be enormous for civilian, strategic satellite communication systems or scientific deep space missions. FPGA technology enables realization of advanced reconfigurable computing platforms which add flexibility in frequency, spectrum, coverage, power etc. These flexibilities not only serve value addition to communication payloads but also fruitful for scientific mission which calls for contingency plans on-boards. FPGA technology also mitigates several on-board anomalies and avert catastrophe of critical missions. Proven its capability in Digital Signal Processing, Image Processing applications, FPGA is found to be very promising for power electronics and control applications too. This paper explores conceptualization, design and implementation of FPGA based digitally controlled EPCs for new generation Flexible SSPAs. The implementation includes advanced Digital Pulse Width Modulator (DPWM) and Digital PID Controller (DPID) algorithms using VHDL/Verilog targeting a robust RTSX FPGA. The FPGA implementation is done in EPC targeting "DC power processing requirement of EPC" "RF power processing of SSPA".*

I. INTRODUCTION

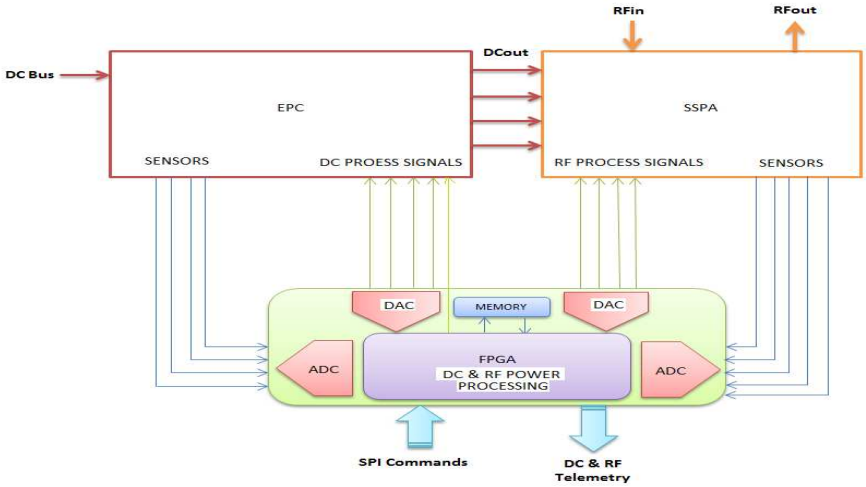
Spacecraft designs are strongly influenced by the learning curves and heritages. Inhibitions are there in adapting new technologies due to huge efforts involved in validating those designs for zero defect operations during mission life of more than 12years. Inducting new designs or technologies without proper evaluation represents unacceptable risks for critical missions and invites surprise or catastrophe at the crucial time of launch or during in-orbit service. Performance degradation, technical glitch or nuisance trip offs during satellite service not only call for ire from the user community but incur commercial loss and cause decline of reputation for satellite manufacturers as well as service providers. So, space community fundamentally lean and focused to conventional and robust approaches with more heritage than new and complex designs. However state of the art performances in efficiency and mass drive the space technologies as the launch cost is driven from mass and size of payloads. Recently flexibilities and re-configurabilities of systems on-board are considered a prime requirement due to uncertainties in the final operational service, user potential and business model (such things often incorrectly forecasted). So satellite service providers insist for payload flexibilities which enable reconfiguration of the payload after launch. This feature is essential for contingencies during deep space missions too. In view of this, spacecraft manufacturers endeavours in validating and inducting new technologies which enable flexibilities and re-configurabilities to keep pace with global technology & business trends.

The Amplifier system for satellite applications, Solid State Power Amplifier (SSPA) consists of an RF chain viz. a preamplifier, driver amplifier and a power amplifier. Electronic Power Conditioners (EPC) is one of its constituent which energizes SSPA from an unregulated spacecraft bus. The SSPA technology for space applications are highly driven by the performances like efficiency, linearity and mass. But due to the recent trends in flexible payload architectures and stringent space program schedules more flexibilities, scalability, modularity, re-configurability etc are considered as plus points

II. DESCRIPTION OF THE WORK

This paper presents conceptualization, design and implementation of FPGA based digitally controlled EPCs for new generation flexible satellite payloads (exclusively for Flexible 15W SSPA). The functional block diagram is as shown in following section. This design is done such that an FPGA sitting inside EPC can facilitate "DC power management of EPC" as well as "RF power management of SSPA. Apart from that, it does the health monitoring and protection aspects of both source and load. The same concept can be implemented in any other RF loads like Receivers, LNA, Up/Down converters or Optical, Electro-Mechanical, Digital loads of various payloads. In a typical SSPA (RF load) application, EPC-DC power management like PWM signal generation, PID controls, output sequencing, soft-start, protections, Reference voltage, switching frequency, ZVS/ZCS signals, LDO controls etc. and SSPA-RF power management like Fixed Bias, Dynamic Bias, Envelope Tracking Modes or with Gain-Phase-Compression-efficiency tracking features or temperature compensation,

BOA/ALC controls, DC/RF telemetries etc. These features are ideal for new generation "Flexible SSPAs" targeting flexibilities in RF power, Bandwidth and Coverage.



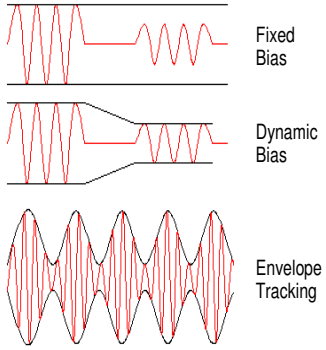


FIG.1 (a) Conceptualized FPGA based EPC for FLEX-SSPA FIG.1 (b) SSPA Features targeted

Two potential dc-dc converters widely used for space applications viz. Active Clamp Forward and ZVT Phase-shift full-bridge converters as shown in fig.2 are identified for FPGA implementation.

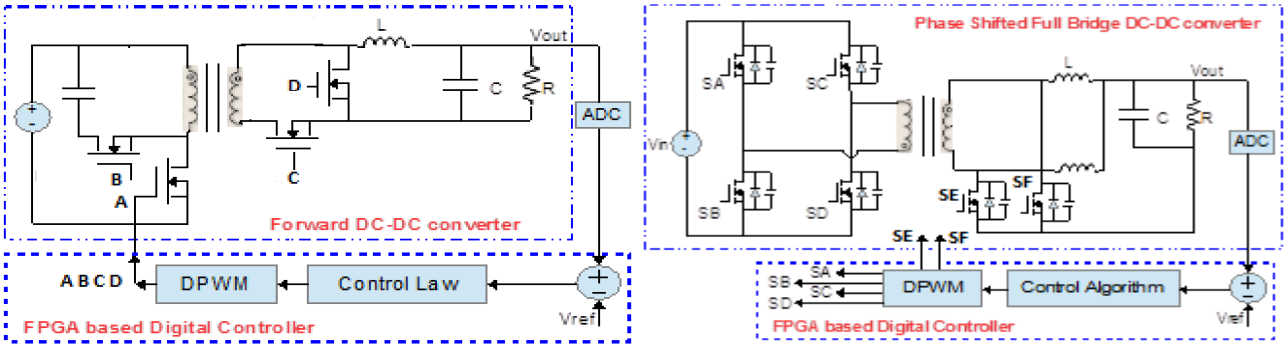


FIG.2 ImplementedFPGA based(a) Forward converter (b) Phase Shifted Full Bridge converter

III. ANALOG CONTROL VERSES DIGITAL CONTROL

Historically analog control based linear and switch based mode power conversions technologies were used in space, for even up to recent years. Invasion of digital electronics enabled engineers to try experimental power systems to en-cash flexibilities and changing configurations. A comparison of analog verses digital control is given below

Advantages of digital control:

- Bring in flexibility, re-configurability
- Digital components are less susceptible to aging and environmental variations.
- They are less sensitive to noise.
- Changing a function does not require an alteration in the hardware.
- Improved sensitivity to parameter variations.

Disadvantages of digital control:

- Complex design and analysis required to realize stable digital control systems
- Signal resolution due to finite word length of the digital processor.
- Limit cycle oscillation.
- Time delays in control loop due to the computation of control algorithm by the processor.

Digital control paves way for implementing advanced control functions; improve communication & coordination among various systems etc. High speed digital components Microcontrollers (MCU), Digital Signal Processor (DSP) and flexible software-solutions using these devices were flourished in the last few decades. Recent trend is towards programmable hardware-solutions using CPLD, FPGA and ASIC like devices. Indeed, these generic components combine high speed and re-programmable solutions with software tools for evaluation and implementation with high integration density. FPGA is a potential device for space due to following reasons

- FPGA are compact, reliable & now available in radiation-hardened, making it attractive for space flights.
- FPGA can be programmed easily in hardware & software
- FPGA has superior speed and capacity
- FPGA allow most functions of control & communication
- FPGA can be integrated on a single chip, System On Chip, can be easily migrated to ASIC

FPGA could be the most potential digital device for space applications due to the very nature of space, i.e. unpredictable environments. Re-configurability features are very promising for deep space or inter planetary missions like Lander / Rover reconfigured from ground. As there are ambiguities in prediction of location where Lander is landed (well or hill-top) navigation, sun-tracking, MPPT algorithms can be uploaded from ground after analysing Lander/Rover camera images. FPGA device can mitigate on-board anomalies in critical space missions too. Digital control using FPGAs can provides advantages viz. automatic and commendable operating points, parameters, high speed/complex algorithms implementation, optimizations, compensate against component variations or degradations with aging, communication within system and among systems.Potential advantages of digital controller implementation include much improved flexibility, reduced design time, programmability, elimination of discrete tuning components, improved system reliability, easier system integration, and possibility to include various performance enhancements. Also it brings the opportunity to realize non-linear, predictive and adaptive control strategies provides a strong reason why digital control could yield worthwhile advantages

IV. DIGITAL CONTROL CHALLENGES, CRITICALITIES

Analog control provides very fine resolution for output voltage adjustment limited by finite loop gain, thermal effects and system noise. On the other hand, a digital control loop has a finite set of discrete “set points” resulting from the resolution of “quantizing elements”, ADC, DPID & DPWM. However if judiciously designed, digital systems can beat analog system output accuracy, ripple, close loop and efficiency performances. In analog control, PWM signals are generated by “ramp” whereas in digital “calculated, digitally counted ramp” is used. Similarly analog control need a PID/compensator for close loop gain-phase margins loop where as in digital controlled systems, digital PID/ Controller for the same with additional phase shift from digital processing. The static and dynamic output voltage regulation capabilities in digital control depend on the characteristics of the ADC resolution, the discrete set of duty ratios and ultimately the discrete set of achievable output voltages depends on the DPWM resolution. If the resolution of ADC and DPWM is not sufficiently high, an undesirable limit-cycle oscillation may occur. The requirement for a high-resolution ADC and DPWM is an important consideration in the realization of digitally controlled EPC.It has been observed and analysed that a large-magnitude limit-cycle oscillation might happen at the output voltage if Vo_DPWM is not as fine as that of the ADC, VADC, i.e.,

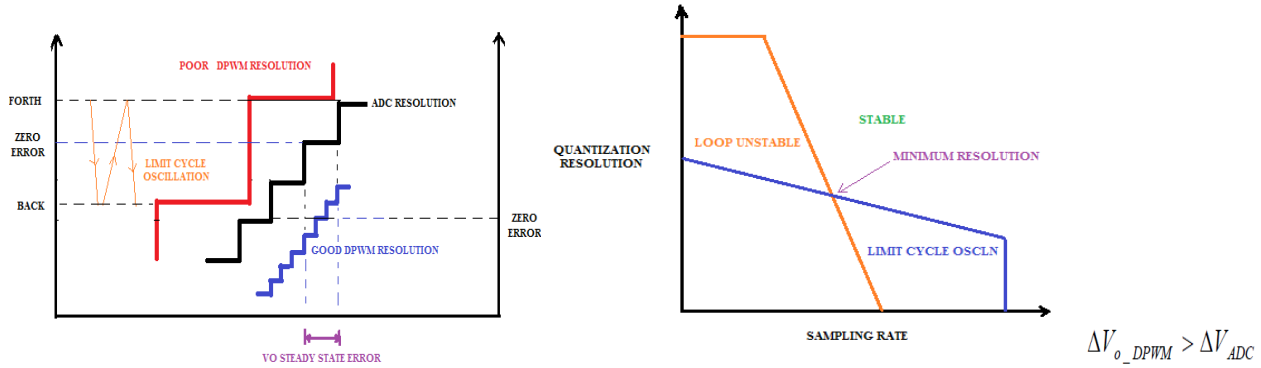


FIG.3 (a) Limit cycle oscillation: A graphical representation (b) Optimization philosophy, stability crieteria

In steady state, the controller will be attempting to drive Vout to the zero-error bin,however due to the lack of a DPWM level there; it will alternate between the DPWM levels around the zero-error bin. These results in non-equilibrium behaviour, such

as steady-state limit cycling.The first step towards eliminating limit cycles is to ensure that under all circumstances there is a DPWM level that maps into the zero-error bin. This can be guaranteed if the resolution of the DPWM module is finer than the resolution of the ADC

V. DIGITAL CONTROL ELEMENTS & ARCHITECTURES

A. DPWM Architectures

High resolution DPWM is then the key module to restrain the undesired limit cycle oscillation. Two DPWM algorithms (Counter-comparator & Sigma-delta) were explored for implementation of Forward Converter and PSFB converter. Counter-comparator selected based on simplicity/linearity advantage for implementation in low switching frequency applications (<500 KHz) whereas Sigma-delta selected based up on better noise rejection characteristics implementing in high switching freq. applications (>500 KHz)

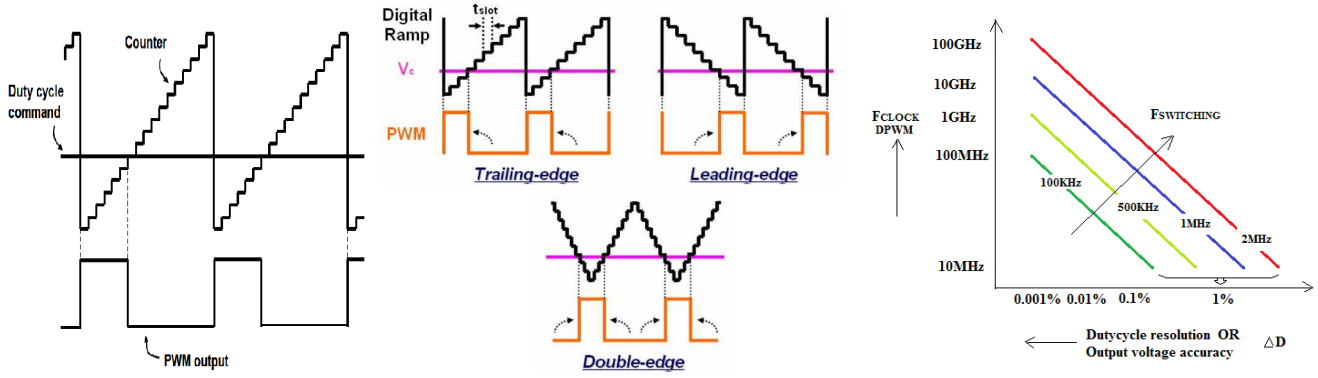


FIG.4(a) Counter-Comparator DPWM(b) Various schemes of Counter-Comparator DPWM **(c)** Vo accuracy verses Fclock-DPWM

Similar to the analog PWM, the DPWM functions utilize a control signal, Vc, to compare with the PWM ramp. Becauseof the advantages of sampling with double-edge modulation, ithas been widely used in the industry applications. The implementation difference from trailing-edge and leading edgeschemes is that it has both the rising& falling digital ramp.

Fig.4(c) shows relationship between duty cycle and required DPWM clock frequency under different switching frequencies. If a 10mV output resolution is desired with 10V input for the buck converter, a 0.1% duty cycle resolution is required. As a result, if the switching frequency is 100 kHz, a 20MHz system clock is needed for DPWM. If the switching frequency is 2 MHz, a1GHz system clock is needed. Therefore, in the applications that require both tight output regulation and high switching frequency, such as voltage regulators or other point-of-load converters, high DPWM resolution is one of the major concerns for the digital power controller designers. Many architectures are proposed since 1997, such as delay line, sigma-delta and hysteretic modules, etc. Sigma-delta type can achieve high resolution without high bits of DPWM, but suffers from the problem of poor transient response. Hystereticmodule is easy to implement and can reach high resolution, however its switching frequency is not constant. Delay line types are popular for its simplicity. Hybrid DPWM can achieve high resolution without taking very large die size. In order to optimize circuit resources in terms of occupied area and power consumption, a general architecture based on tapped delay lines is proposed, which includes segmentation of the input digital code to drive binary weighted delay cells and thermo-meter decoded unary delay cells

B. ADC Architectures

A wide choice of ADC architectures exist that differ in resolution, bandwidth, accuracy, and power requirements. If the sampling rate is much faster than the plant dynamics, the control looks like continuous time to the plant.

C. DPID Architectures

Achieving high accuracy of output voltage using advanced ADC architectures and DPWM schemes is only one part of the digital control. The most important part is advanced Proportional-Integral-Derivative (PID) control laws; especially as it breaks bandwidth limitations of analog control. Type III compensator implemented in this project is shown

A COMPARISON OF VARIOUS ARCHITECTURES OF DPWM, ADC & DPID

TABLE I

DPWM Architectures performance comparison			
Architecture	***Si Area***	***Power Consumption***	***Accuracy***
Counter-comparator	Low	High	High
Delay-line	High	Medium	Medium
Hybrid delay-line	Medium	Medium	Medium
Segmented delay-line	Low	Low	Low
Ring-oscillator	High	Medium	Medium
Segmented ring osclr	Low	Low	Low
Digital-dither	Low	Low	Medium
Sigma-delta	Low	Low	Medium

ADC Architectures performance comparison				
Architecture	***Speed***	***Cost***	***Power***	***Accuracy***
Flash ADC	Medium	High	High	High
Delay-line ADC	High	Medium	Medium	Medium
Ring-oscillator ADC	Medium	High	Medium	Medium

DPID Architectures performance comparison				
TYPE	***Algorithm***	***Complexity***	***Speed***	***Accuracy***
PID	Fixed/Self-Tuning	Low	High	Low
Compensator	Fixed/Adaptive Type I,II,III	Medium	Medium	Medium
Controller	Predictive, Robust (GA, FUZZY, SM, AI)	High	Medium	High

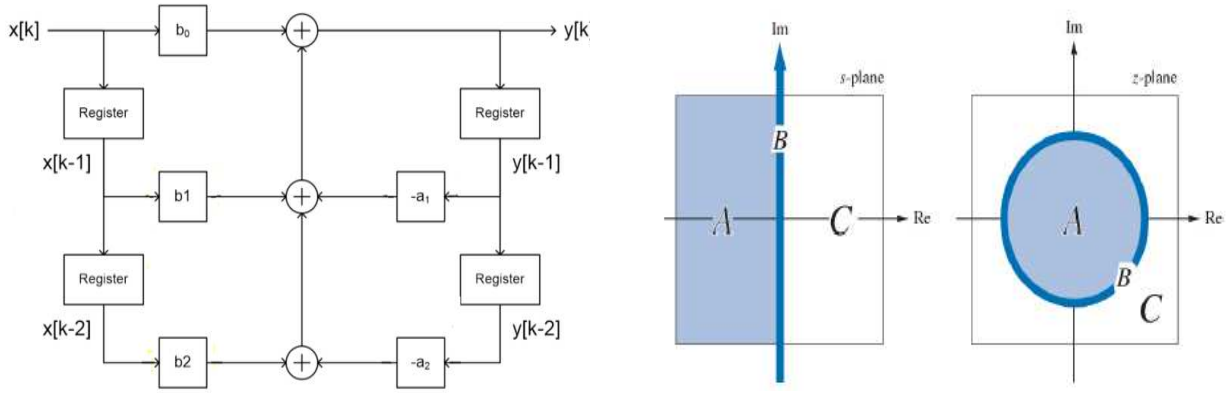


Fig.5 (a) TYPE III DPID Structure Implemented (b) S-Plane to Z-Planetransform and stability criteria, regionA

VI. DIGITAL CONTROL MODELLING

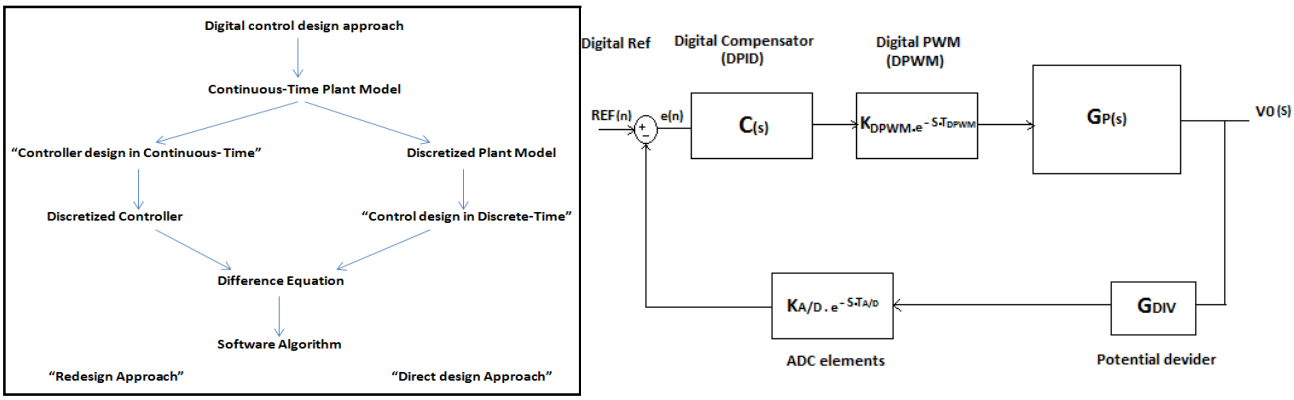


Fig.6 (a) Digital close loop design philosophy (b) Digitalclose loop model

EQUATIONS

FPGA based digital control loop modelling using a digital re-design approach is illustrated as below.Resolution requirements of ADC & DPWM are calculated as

$$N_{ADC} \geq Int[Log_2(\frac{V_{MAX}.V_{OUT}}{V_{REF}.\Delta V})] \; N_{DPWM\ ]} \geq Int[N_{ADC} + Log_2(\frac{V_{REF}}{V_{MAX}.D})]$$

$$N_{DPWM} \geq N_{ADC} + 1 \; F_{CLOCK} \geq 2^{N_{DPWM}}.F_{SW} \quad \Delta D = \frac{F_{SW}}{F_{CLOCK}} = \frac{1}{2^{N_{DPWM}}}$$

Plant transfer function forward conv. derived as

$$G_P(s) = \frac{V_{in}.n.D.R_L.(s.C_o.R_{ESR} + 1)}{s^2.L_o.C_o.\left(1 + \frac{R_{ESR}}{R_L}\right) + s.\left(\frac{L_o}{R_L} + C_o.R_{ESR}\right) + 1}$$

Plant transfer function PSFB converter derived as

$$G_P(s) = \frac{V_{in}.n.Deff.R_L.(s.C_o.R_{ESR} + 1)}{s^2.L_o.C_o.\left(1 + \frac{R_{ESR}}{R_L}\right) + s.\left(\frac{L_o}{R_L} + C_o.R_{ESR}\right) + 1} \quad G_{A/D}(s) = K_{A/D}.e^{-s*t_{A/D}} \; G_{DPWM}(s) = K_{DPWM}.e^{-s*t_{DPWM}}$$

System transfer function $G_{OVERALL}(s) = G_P(s).G_{DIV}.G_{A/D}(s).G_{DPWM}(s).C(s)$

Continuous C(s) to Discrete C(z) transformation can be done using Euler method, Tustin bilinear transformation method or Pole-Zero matching method. We have used Tustin bilinear transformation due to better accuracy, with help of Matlab.Final implemented DPID controller structure

$$C(z) = \frac{Y(z)}{X(z)} = \frac{b0 + b1.z^{-1} + b2.z^{-2}}{1 + a1.z^{-1} + a2.z^{-2}}$$

This is translated into following difference equation, aprogrammable form with digital coefficients B0, B1, B2, A1 and A2 are tuned for stability

$$Y_{(n)} = B_0.X_{(n)} + B_1.X_{(n-1)} + B_2.X_{(n-2)} - A_1.Y_{(n-1)} - A_2.Y_{(n-2)}$$

VII. DIGITAL IMPLEMENTATION

There are mainly three different types of FPGAs: SRAM, Flash, and Antifuse-based FPGAs.The different characteristics with respect to processing capabilities and robustness in radiation performances are analyzed for FPGA devices from various manufacturers like ACTEL (Microsemi), Xilinx, Atmel etc. Out of this we have selected Actel's RTSX-SU family's RTSX32SU-CQ84 FPGA. This device is found optimum for meeting the functional requirements with minimum footprint when embed in a DC-DC converter card. Due to one-time programmability and high cost rad hard RTAX-S/RTSX devices, prototyping using the traditional approach (uses the same space grade device) may be costly. Using ProASIC3E FPGA flash-based programming technology provides significant advantages, such as non-volatile re-programmability with easier technology mapping and Netlist optimizations. Aldec prototyping adaptor board maps the footprint of the Actel ProASIC3E FPGA device to the footprint of the Actel RTAXor RTSX device.ActelLibero/Quartustool used for VHDL programming.

vendor	XILINX		Microsemi / Actel		ATMEL
Device type datasheet	QPro™ Virtex™-II	Virtex-5QV	RTproASIC3	RTAX-S/SL	AT40KEL040
TID (Krads(Si))	200	>1000	>100; >45 if reprogramming	300	300
SEL (MeV/mg/cm2)	> 160	>125	>64	> 117	80
SEU sat cross section (cm2/bit) Or GEO (Errors/Bit-Day)	GEO upsets < 1.5E-6 per device day (with TMR+ SRAM scrubbing)	Conf. bits 4.85 Upsets/Device/Year ; SEFI static 9,930 U/D/Y BlockRAM - 2.5E 11 U/D/D ; dynamic blocks ~2.7E-4 U/b/day	2E-7 cm² per flip-flop; 4E-8 cm² per SRAM memory bit; none for FLASH	< 1E-10 Worst-Case GEO	2.5E-8 (*) 2.5E-7 (**)
SEU LE I th (MeV/mg/cm2)		Very low	>96 (FLASH), >6(FF), >1(SRAM)	>37	16 (*) 15 (**)
SET			2E-6 cm² per global clock network, per IO bank, low LETth	No Anomalies up to 150 MHz	As MH1RT ASICs

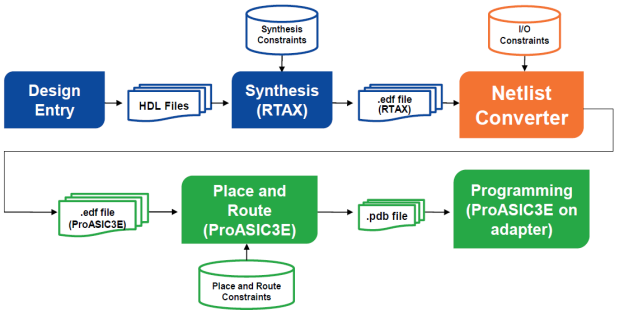


Fig.7 (a) Space grade FPGA device comparison (b) Prototyping method using Aldec adapter/ProAsic3

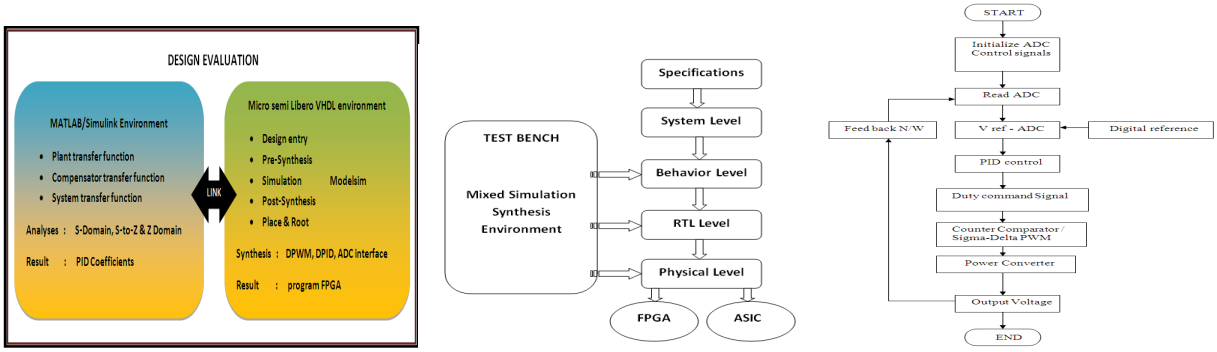
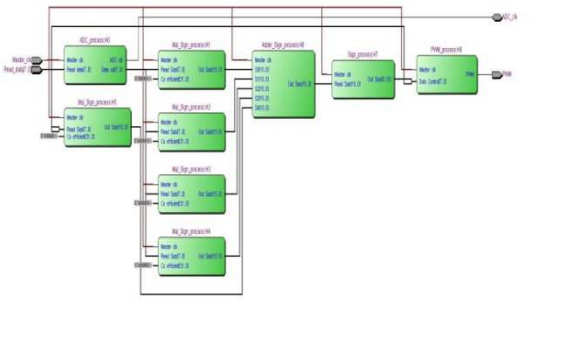
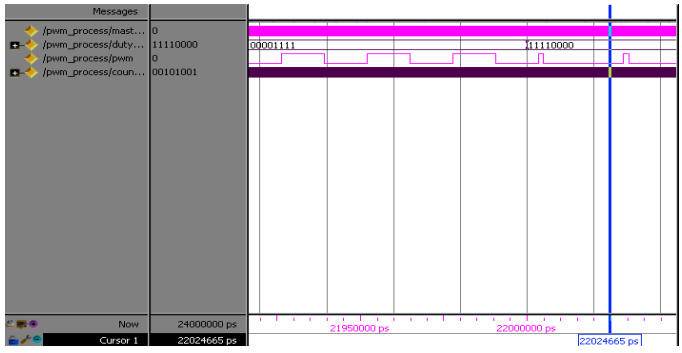


Fig.8 (a) Simulation/synthesis platform (b) Hierarchical Flow / HDL Environment (c) Flow chart of converter loop





------ADC----------DPID----------DPWM------

Fig.9 (a)VHDL Implementation ADC+DPID+DPWM (b) Implementation of DPWM (Forward converter)

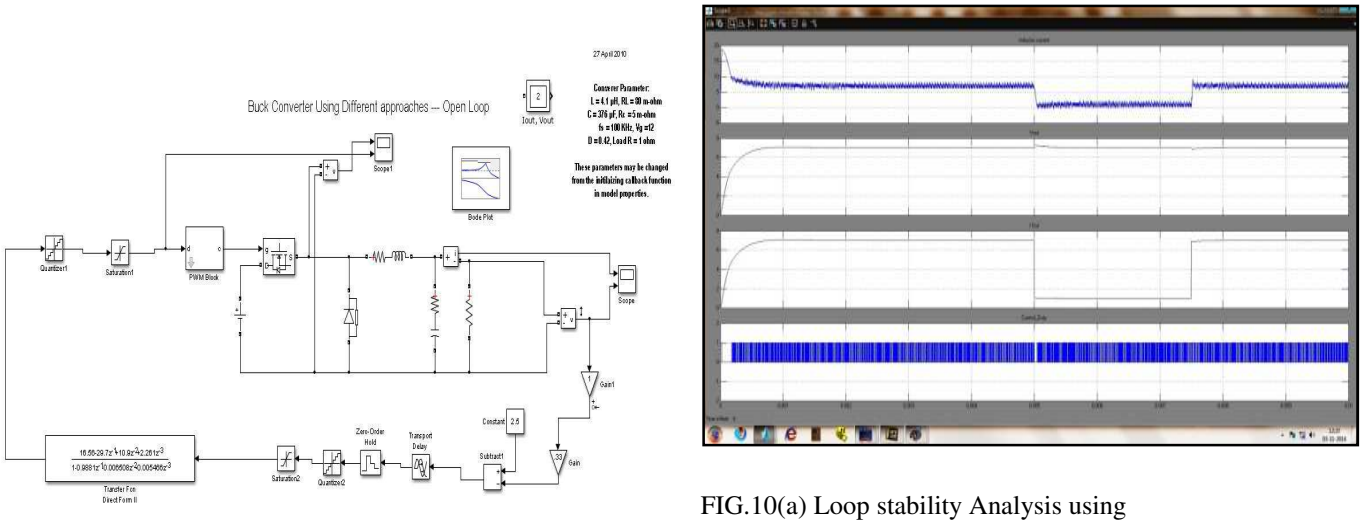


FIG.10(a) Loop stability Analysis using MATLAB/Simulink (b) Start-up, steady-state & load transient simulation results

VIII. RESULTS AND DISCUSSIONS

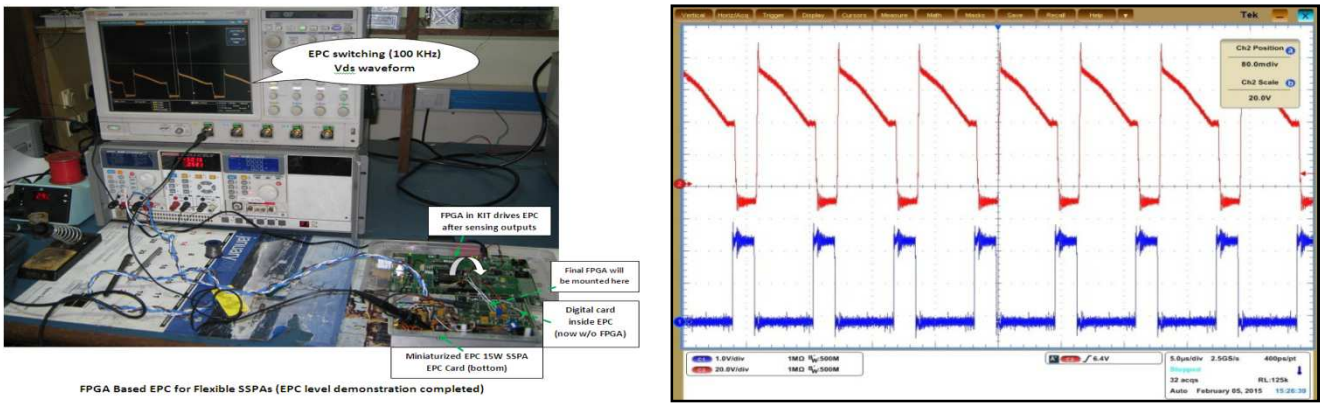


FIG.11 (a) Photograph of FPGA Based EPC for 15W SSPA (b) Waveforms VDS, VGS captured in FPGA based EPC

IX. CONCLUSION

Benefits of digital control in power electronics are not limited to power processing of dc power systems but to the load which it is connected to, viz. RF/Optical/Electro-mechanical systems etc. FPGA Based EPCs has potential for new generation flexible payload realization. The proof concept implemented in an EPC for 15W SSPA, output flexibilities verified with SPI commands. The performances were found satisfactory.The reach of such power embedded system could be Microsatellites, ISS or Deep space mission lander/rover systems

Acknowledgment

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